(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 005 204 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
31.05.2000 Bulletin 2000/22

(51) Int. Cl.[7]: H04L 27/26

(21) Application number: 99123430.3

(22) Date of filing: 24.11.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 26.11.1998 JP 33611198
24.03.1999 JP 7957499

(71) Applicant:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka 571-8501 (JP)

(72) Inventor: Sudo, Hiroaki
Yokohama-shi, Kanagawa 224-0054 (JP)

(74) Representative:
Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Symbol synchronization in an OFDM receiver

(57) Multiplier 103 calculates the correlation value of the received signal with the one-symbol-delayed received signal, integrator 104 integrates the calculated correlation value, subtracter 105 executes subtract processing between the integrated value and an arbitrary threshold level, and decider 106 decides a level of the resultant, fastest timing detection section 107 compares the peak detected timing for each of a plurality of frames received during a predetermined time to each other to select the fastest peak detected timing, and using the selected timing as a processing initiation timing, FFT circuit 108 executes FFT processing on the received signal.

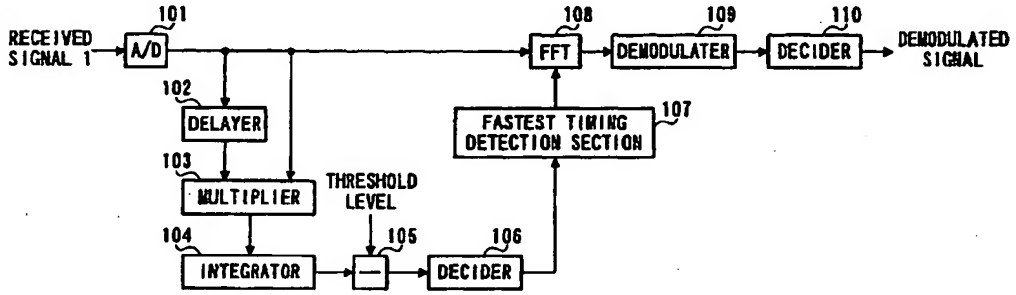


FIG. 5

EP 1 005 204 A2

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an OFDM (Orthogonal Frequency Division Multiplexing) reception apparatus, and more particularly, to an OPDM reception apparatus in a mobile communication and a symbol synchronization error reduction method therefor.

Description of the Related Art

[0002] A conventional OFDM reception apparatus is explained below using FIG.1 to FIG.4. FIG.1 is a schematic block diagram illustrating a part of a configuration of the conventional OFDM reception apparatus. FIG.2 is a schematic block diagram illustrating a part of another configuration of the conventional OFDM reception apparatus. FIG.3 is a schematic diagram illustrating a frame structure of a transmission signal in an OFDM system. FIG.4 is a schematic diagram illustrating a correlation value calculation result in the OFDM reception apparatus.

[0003] The configuration of the conventional OFDM reception apparatus and an acquisition method for symbol synchronization timing therein are explained first using FIG.1.

[0004] In FIG.1, A/D converter 1 converts a received signal from an analog signal to a digital signal. Delayer 2 delays the received signal which is converted into the digital signal (hereinafter, also referred to as received digital signal) by one symbol. Multiplier 3 executes complex multiplication processing between the received digital signal and the received signal delayed by one symbol in delayer 2 (hereinafter, also referred to as one-symbol-delayed received signal).

[0005] Integrator 4 integrates outputs from multiplier 3. Subtracter 5 processes the subtraction between an output from integrator 4 and a threshold level. Decider 6 decides whether an output from subtracter 5 is positive or negative. For example, in the case where such an output is positive, it is determined that the integrated result exceeds the threshold level, and the timing having such an integrated result is used as a processing timing for FFT which is descried below.

[0006] FFT circuit 7 executes fast Fourier transform (FFT) processing on the received digital signal. The FFT processing in FFT circuit 7 is initiated based on an output from decider 6, i.e., the processing initiation timing.

[0007] Demodulator 8 executes demodulation processing on an output signal from FFT circuit 7. Decider 9 executes a decision on an output signal from demodulator 8.

[0008] Operations in the OFDM reception apparatus with the configuration as described above are next explained. The received signal generally has a frame structure as illustrated in FIG.3. In such a e frame structure, guard interval 42, with the same signal as the end portion of effective symbols, is provided before effective symbol 41 for the purpose of canceling a delayed version, and phase reference symbol (pilot symbol) 43 and synchronization symbol 44, which is the same signal as phase reference symbol 43, are provided at the head of signals (before the guard interval).

[0009] The received signal, which is converted into the digital signal in A/D converter 1, is delayed by one symbol in delayer 2. Multiplier 3 obtains the correlation value of the received signal with the one-symbol-delayed received signal.

[0010] Since the same signal as phase reference symbol 43 is provided as synchronization symbol 44 before phase reference symbol 43, as illustrated in FIG.4, the correlation value calculated in multiplier 3 has the peak at a position which is the end portion of the phase reference symbol of the received signal and the end portion of the synchronization symbol of the one-symbol-delayed signal (head of phase reference symbol 43). Therefore, by the use of subtracter 5 and decider 6, it is possible to detect the peak of the correlation value by comparing the output from integrator 4 to the threshold level.

[0011] The symbol synchronization timing, which is an output from decider 6, is input to FFT circuit 7 as a FFT processing initiation trigger.

[0012] The received signal subjected to the FFT processing in FFT circuit 7 is output to demodulator 8 to be demodulated therein, and then decided in decider 9 to be a demodulated signal.

[0013] The case where the diversity is performed on received signals from a plurality of branches is next described using FIG.2.

[0014] In FIG.2, A/D converters 11 and 12 respectively convert received signal 1 from branch 1 and received signal 2 from branch 2 each from the analog signal to the digital signal. Delayers 13 and 14 respectively delay received digital signals 1 and 2 each by one symbol. Multipliers 15 and 16 execute complex multiplication processing between received digital signals 1 and 2, and received signals 1 and 2 which are delayed by one symbol in delayers 403 and 404, respectively.

[0015] Integrators 17 and 18 integrate respective outputs from multipliers 15 and 16. Subtracters 17 and 18 execute subtraction processing between respective outputs from integrators 17 and 18 and a threshold level. Deciders 21 and 22 decide whether respective outputs from subtracters 19 and 20 are positive or negative. For example, in the case where such an output is positive, it is determined that the integrated result exceeds the threshold level, and the timing having such an integrated result is used as a processing timing for FFT which is descried below.

[0016] FFT circuits 23 and 24 execute respectively fast Fourier transform (FFT) processing on received dig-

BNSDOCID: <EP_____1005204A2_I_>

ital signals 1 and 2. The FFT processing in FFT circuits 23 and 24 is initiated based on respective outputs from deciders 21 and 22, i.e., the processing initiation timing.

[0017] Selector 25 selects an output from FFT circuit 23 or 24 to output corresponding to received levels of received signals 1 and 2. Demodulator 26 demodulates an output signal from selector 25. Decider 27 executes a decision on an output signal from demodulator 26.

[0018] Arc tangent calculators 28 and 29 execute arc tangent calculation on respective output signals from integrators 17 and 18. Averager 30 averages outputs from arc tangent calculators 28 and 29.

[0019] Operations in the OFDM reception apparatus with the configuration as described above are next explained.

[0020] Received signals 1 and 2 received in branches 1 and 2 are converted into digital signals in A/D converters 11 and 12, and then are delayed each by one symbol in delayers 13 and 14, respectively. Multipliers 15 and 16 obtain the correlation values of the respective received signals with the respective one-symbol-delayed received signals.

[0021] With respect to the correlation values calculated for the received signals in respective branches, by the use of subtracters 19 and 20, and deciders 21 and 22, respectively, the peaks are detected by comparing respective outputs from multipliers 17 and 18 to a threshold level.

[0022] The symbol synchronization timings, which are the outputs from deciders 21 and 22, are input to FFT circuits 23 and 24, respectively, each as a FFT processing initiation trigger.

[0023] With respect to received signals 1 and 2 subjected to the FFT processing in FFT circuits 23 and 24, selector 25 selects either of received signal 1 or 2, of which the received level is higher than the other, to output to demodulator 26. The received signal, which is selected in selector 25 and input to demodulator 26, is demodulated in demodulator 26, and then decided in decider 27 to be a demodulated signal.

[0024] On the other hand, output signals from integrators 17 and 18 are subjected to arc tangent calculation respectively in arc tangent calculators 28 and 29, so as to calculate respective phase rotation amounts of received signals in respective branches. Averager 30 averages the respective phase rotation amounts of received signals in respective branches to output. Phase rotation amount Δf, which is an output from averager 30, is used as a frequency offset amount to be compensated in the frequency offset compensation in the quasi-coherent detection.

[0025] As descried above, the conventional OFDM reception apparatus calculates the correlation value of the received signal with the one-symbol-delayed received signal, detects the peak of the correlation value, and obtains the timing, at which the peak is detected, as the symbol synchronization timing, which is used as the timing for FFT processing initiation for the received signal. Further, in the diversity, the branch with the highest received level is selected.

[0026] However, in the conventional OFDM reception apparatus, there is a problem that error rate characteristics deteriorate greatly under multipath environments where the symbol synchronization timing tends to be acquired behind an actual timing.

[0027] In other words, in the conventional OFDM reception apparatus, since the guard interval is proved before the effective symbols, the effective symbols are extracted without any problems in the case where the symbol synchronization timing is acquired faster than the actual timing. However, in the case where the synchronization is acquired at a timing slower than the actual timing, interference occurs and the error rate characteristics deteriorate greatly.

SUMMARY OF THE INVENTION

[0028] An object of the present invention is to provide an OFDM reception apparatus which improves the accuracy for the symbol synchronization acquisition, and further improves the error rate under multipath environments.

[0029] A gist of the present invention is to use the peak detected timing for a frame of which the peak of the correlation value is detected fastest among a plurality of frames received during a predetermined time, as the symbol synchronization timing which is the timing for FFT processing initiation, and in the diversity, to use the peak detected timing for a received signal in a branch of which the peak of the correlation value is detected fastest among all received signals, as the symbol synchronization timing which is the timing for FFT processing initiation common to received signals in all branches.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The above and other objects and features of the invention will appear more fully hereinafter from a consideration of the following description taken in connection with the accompanying drawing wherein one example is illustrated by way of example, in which;

FIG.1 is a schematic block diagram illustrating a part of a configuration of a conventional OFDM reception apparatus;

FIG.2 is a schematic block diagram illustrating a part of another configuration of the conventional OFDM reception apparatus;

FIG.3 is a schematic diagram illustrating a frame structure of a transmission signal in an OFDM system;

FIG.4 is a schematic diagram illustrating a correlation value calculation result in the OFDM reception apparatus;

EPNSDOCID: <EP_____1005204A2_I_>

FIG.5 is a schematic block diagram illustrating a part of a configuration of an OFDM reception apparatus according to a first embodiment of the present invention;

FIG.6 is a schematic block diagram illustrating a part of a configuration of a fastest timing detection section in the OFDM reception apparatus according to the first embodiment of the present invention;

FIG.7 is a schematic diagram illustrating a part of a configuration of a fastest timing detection section in the OFDM reception apparatus according to the second embodiment of the present invention;

FIG.8 is a schematic block diagram illustrating a part of a configuration of an OFDM reception apparatus according to a third embodiment of the present invention;

FIG.9 is a schematic block diagram illustrating a part of a configuration of a fastest timing detection section in the OFDM reception apparatus according to the third embodiment of the present invention;

FIG.10 is a schematic block diagram illustrating a part of a configuration of an OFDM reception apparatus according to a fourth embodiment of the present invention; and

FIG.11 is a schematic block diagram illustrating a part of a configuration of an OFDM reception apparatus according to a fifth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Embodiments of the present invention are described specifically below with reference to drawings.

(First embodiment)

[0032] An OFDM reception apparatus according to this embodiment uses, as the symbol synchronization timing, the timing for a frame of which the symbol synchronization is acquired at the fastest timing among a plurality of frames received during a predetermined time.

[0033] The OFDM reception apparatus according to this embodiment is explained below using FIG.5 and FIG.6. FIG.5 is a schematic block diagram illustrating a part of a configuration of the OFDM reception apparatus according to the first embodiment of the present invention, and FIG.6 is a schematic block diagram illustrating a part of a configuration of a fastest timing detection section in the OFDM reception apparatus according to the first embodiment of the present invention.

[0034] A/D converter 101 converts a received signal from an analog signal to a digital signal. Delayer 102 delays the received signal which is converted into the digital signal by one symbol. Multiplier 103 executes complex multiplication processing between the received digital signal and the received signal delayed by one symbol in delayer 102.

[0035] Integrator 104 integrates outputs from multiplier 103. Subtracter 105 processes the subtraction between an output from integrator 104 and a threshold level. Decider 106 decides whether an output from subtracter 105 is positive or negative. For example, in the case where such an output is positive, it is determined that the integrated result exceeds the threshold level, and the timing having such an integrated result is used as a processing timing for FFT which is descried below.

[0036] With respect to a plurality of frames received during a predetermined time, fastest timing detection section 107 compares outputs from decider 106, selects a frame of which the peak of the correlation value is detected at the fastest timing, and outputs the peak timing of the selected frame as the symbol synchronization timing to FFT circuit 108. In addition, the above-mentioned predetermined time is determined arbitrary. Fastest timing detection section 107 is described specifically later.

[0037] FFT circuit 108 executes fast Fourier transform (FFT) processing on the received digital signal. The FFT processing in FFT circuit 108 is initiated based on an output from fastest timing detection section 107, i.e., the processing initiation timing.

[0038] Demodulator 109 executes demodulation processing on an output signal from FFT circuit 108. Decider 110 executes a decision on an output signal from demodulator 109.

[0039] Fastest timing detection section 107 is next described specifically using FIG.6.

[0040] Fastest timing detection section 107 is, As illustrated in FIG.6, composed of counter 201, switch 202, a plurality of memories 203, and comparator 204.

[0041] Counter 201 has an operation period equal to a frame length, suspends the counting operation at the peak detected timing for each frame of the received signal, which is output from decider 106, and holds the counted numerical value obtained at the suspended time.

[0042] Switch 202 switches the counted numerical value for each frame to output to respective different memory 203.

[0043] Each memory 203 stores the counted numerical value for respective frame. The number of memories 203 is determined so as to enable the storage of the number of frames received during a predetermined time which is directed by fastest timing detection section 107. For example, when it is assumed that the predetermined time directed by fastest timing detection section is 1 msec, and that average 4 frames are received during 1 msec, the number of memories 203 to be provided is equal to or more than 4.

[0044] Comparator 204 reads counted numerical values for respective frames stored in respective memories 203 to compare, and outputs the least numerical value thereamong. The counted value output from comparator 204 is used as the symbol synchronization tim-

BNSDOCID: <EP_____1005204A2_I_>

ing, and further as the FFT processing initiation timing.

[0045] Operations in the OFDM reception apparatus with the configuration as described above are next explained.

[0046] The received signal is converted into the digital signal in A/D converter 101, and then delayed by one symbol in delayer 102. Multiplier 103 calculates the correlation value of the received signal with the one-symbol-delayed received signal.

[0047] Integrator 104 integrates the calculated correlation value, subtracter 105 processes the subtraction between the integrated value and the threshold level, and decider 106 executes a decision on the resultant, thus making it possible to detect the peak of the correlation value for each frame of the received signal.

[0048] With respect to the peaks of the correlation values output from decider 106, fastest timing detection section 107 compares the peak detected timing for each of a plurality of frames received during the predetermined time to each other to select the fastest peak detected timing.

[0049] The received signal subjected to A/D conversion is subjected to FFT processing in FFT circuit 108 using the timing output from comparator 204 as the processing initiation timing.

[0050] The received signal subjected to the FFT processing is output to demodulator 109, demodulated in demodulator 109, and decided in decider 110 to be a demodulated signal

[0051] As described above, according to this embodiment, among the timings for the peaks of the correlation values detected for a plurality of frames received during a predetermined time, the fastest timing is used as the symbol synchronization timing, thereby preventing the symbol synchronization timing from being shifted behind the actual timing, and further improving the acquisition accuracy for symbol synchronization timing. As a result, it is possible to improve the error rate under the multipath environments.

(Second embodiment)

[0052] An OFDM reception apparatus according to this embodiment has the same configuration as that in the first embodiment, except a reduced memory capacity in a fastest timing detection section.

[0053] The OFDM reception apparatus according this embodiment is explained below using FIG.7. FIG.7 is a schematic block diagram of a part of a configuration of the fastest timing detection section in the OFDM reception apparatus according to the second embodiment of the present invention. In addition, the same blocks as those in the first embodiment are given the same symbols to omit detailed explanations.

[0054] In FIG.7, counter 201 outputs the counted numerical value for the peak detected timing for each frame of the received signal sequentially in the same way as in the first embodiment.

[0055] Switch 301 outputs, based on an output from comparator 204, either of the counted numerical value counted in counter 201 or that already stored in memory 302, which is smaller than the other, to memory 302 to be stored.

[0056] Comparator 204 compares the counted numerical value stored in memory 302 to that output from counter 201 to output a smaller value.

[0057] As described above, according to this embodiment, whenever the fastest timing appears, the fastest timing detection section stores such a timing to use the symbol synchronization timing, thereby improving the accuracy for the symbol synchronization acquisition, while reducing the memory capacity, and enabling the apparatus to be miniaturized and light-weighted.

[0058] The third to fifth embodiments below describe about the case where the diversity is performed.

(Third embodiment)

[0059] An OFDM reception apparatus according to this embodiment uses the symbol synchronization timing for a received signal in a branch of which the symbol synchronization is acquired at the fastest timing, as the symbol synchronization timing for received signals in all branches,.

[0060] The OFDM reception apparatus according to this embodiment is explained below using FIG.8. FIG.8 is a schematic block diagram illustrating a part of a configuration of the OFDM reception apparatus according to the third embodiment of the present invention.

[0061] A/D converters 401 and 402 respectively convert received signal 1 from branch 1 and received signal 2 from branch 2 each from the analog signal to the digital signal. Delayers 403 and 404 respectively delay received digital signals 1 and 2 each by one symbol. Multipliers 405 and 406 execute complex multiplication processing between received digital signals 1 and 2, and received signals 1 and 2 which are delayed by one symbol in delayers 403 and 404, respectively.

[0062] Integrators 407 and 408 integrate respective outputs from multipliers 405 and 406. Subtracters 409 and 410 execute subtraction processing between respective outputs from integrators 407 and 408 and a threshold level. Deciders 411 and 412 decide whether respective outputs from subtracters 409 and 410 are positive or negative. For example, in the case where such an output is positive, it is determined that the integrated result exceeds the threshold level, and the timing having such an integrated result is used as a processing timing for FFT which is descried below.

[0063] Fastest timing detection section 413 compares an output from decider 411 to an output from decider 412 to select the symbol synchronization timing which is acquired at a faster timing, and outputs the selected timing, as the symbol synchronization timing common to received signals in both branches, to both

BNSDOCID: <EP_____1005204A2_I_>

FFT circuits 414 and 415.

[0064] Fastest timing detection section 413 has counters 501 and 502 which are provided for respective branches, and operate in a predetermined arbitrary period, comparator 503 which compares counted vales by counters 501 and 502, and selector 504 which selects a branch with the smallest counted value.

[0065] FFT circuits 414 and 415 execute respectively fast Fourier transform (FFT) on received digital signals 1 and 2. The FFT processing in FFT circuits 414 and 415 is initiated based on respective outputs from deciders 411 and 412, i.e., the processing initiation timing.

[0066] Selector 416 selects an output from FFT circuit 414 or 415 to output corresponding to received levels of received signals 1 and 2. Demodulator 417 demodulates an output signal from selector 416. Decider 418 executes a decision on an output signal from demodulator 417.

[0067] Arc tangent calculators 419 and 420 execute arc tangent calculation on respective output signals from integrators 407 and 408 in the same way as in conventional case. Averager 421 averages outputs from arc tangent calculators 419 and 420.

[0068] Operations in the OFDM reception apparatus with the configuration as described above are next explained.

[0069] Received signals 1 and 2 received in branches 1 and 2 are converted into digital signals in A/D converters 401 and 402, and then are delayed each by one symbol in delayers 403 and 404, respectively. Multipliers 405 and 406 calculate the correlation values of the respective received signals with the respective one-symbol-delayed received signal.

[0070] Integrators 407 and 408 integrate the calculated correlation values, subtracters 409 and 410 execute subtract processing between the respective integrated values and the threshold level, and deciders 411 and 412 execute a decision on respective resultants, thus making it possible to detect the respective peaks of the correlation values for received signals 1 and 2.

[0071] With respect to the peaks of the correlation values output from deciders 411 and 412, fastest timing detection section 407 compares the timing for the peak to each other to select either one acquired at a faster timing. In other words, in FIG.9, counters 501 and 502 each operates at a sampling rate, and suspends the counting by respective outputs from deciders 411 and 412, and holds the counted numerical value obtained at the suspended time. Comparator 503 compares the numerical value held at the counting suspended time by counter 501 to that by counter 501 to output to selector 504.

[0072] Selector 504 selects an output from decider 411 or 412 for which the counted value held in counter 501 or 502 at the counting suspended time is smaller than the other one, corresponding to an output from comparator 503, so as to output to both FFT circuits 414 and 415.

[0073] The thus selected timing is used as the symbol synchronization timing common to received signals in both branches, i.e., the FFT processing initiation timing common to both FFT circuits 414 and 415 which execute FFT processing respectively on received signals 1 and 2.

[0074] The received digital signals 1 and 2 are subjected to the FFT processing respectively in FFT circuits 414 and 415 using the control signal form fastest timing detection section 413 as a FFT processing initiation trigger.

[0075] With respect to received signals 1 and 2 subjected to the FFT processing, selector 416 selects either of received signal 1 or 2, of which the received level is higher than the other, to output to demodulator 417. The received signal, input to demodulator 417, is demodulated therein, and then decided in decider 418 to be a demodulated signal.

[0076] On the other hand, output signals from integrators 407 and 408 are subjected to arc tangent calculation respectively in arc tangent calculators 419 and 420, so as to calculate respective phase rotation amounts of received signals in respective branches. Averager 421 averages the phase rotation amounts of received signals in respective branches to output. Phase rotation amount Δf, which is an output from averager 421, is used as a frequency offset amount to be compensated in the frequency offset compensation in the quasi-coherent detection.

[0077] As described above, according to this embodiment, the symbol synchronization for a received signal in a branch, which is acquired at the fastest timing, is used as the symbol synchronization timing common to received signals in all branches, thereby preventing the symbol synchronization timing from being shifted behind the actual timing, and further improving the acquisition accuracy for symbol synchronization timing. As a result, it is possible to improve the accuracy for the diversity under the multipath environments.

(Fourth embodiment)

[0078] An OFDM reception apparatus according to this embodiment has almost the same configuration as that in the third embodiment, and uses phase rotation amount Δf of a received signal in a branch of which the symbol synchronization is acquired at the fastest timing.

[0079] The OFDM reception apparatus according this embodiment is explained below using FIG.10. FIG.10 is a schematic block diagram of a part of a configuration of the OFDM reception apparatus according to the fourth embodiment of the present invention. In addition, in FIG.10, the same blocks as those in FIG.8 are given the same symbols to omit detailed explanations.

BNSDOCID: <EP_____1005204A2_I_>

[0080] Selector 601 outputs, based on an output from fastest timing detection section 413, a phase rotation amount of a received signal in a branch of which the symbol synchronization timing is acquired at a faster timing, i.e., either of an output of arc tangent calculator 419 or 420.

[0081] As described above, according to this embodiment, in detecting the frequency offset amount, phase rotation amounts of receives signals in all branches are not averaged, and the phase rotation amount of the received signal in the branch of which the symbol synchronization timing is acquired at a faster timing, which is considered to have a smaller error, is adopted. As a result, it is possible to improve the detection accuracy for the frequency offset amount to be compensated, and to execute accurate frequency offset compensation.

(Fifth embodiment)

[0082] An OFDM reception apparatus according to this embodiment has almost the same configuration as that in the third or fourth embodiment, and adopts an averaged phase rotation amount of received signals in all branches as a frequency offset amount in the case where the symbol synchronization timings for received signals in both branches are close.

[0083] The OFDM reception apparatus according this embodiment is explained below using FIG.11. FIG.11 is a schematic block diagram of a part of a configuration of the OFDM reception apparatus according to the fifth embodiment of the present invention. In addition, the same blocks as those in third or fourth embodiment are given the same symbols to omit detailed explanations.

[0084] When the symbol synchronization timings of received signals in both branches are acquired at close timings, a smaller error is obtained in the case where phase rotation amounts of received signals in both branches are averaged to use like in the third embodiment than in the case where a phase rotation amount of a received signal in either branch is only used like in the fourth embodiment. Therefore, any of such cases is applied corresponding to a time interval between symbol synchronization timings for received signals in both branches.

[0085] Based on a result obtained by comparing acquisition times for symbol synchronization timings for received signals in both branches in fastest timing detection section 413, subtracter 701 subtracts an arbitrary threshold level from the time interval between both timings. Decider 702 decides whether an output from subtracter 701 is positive or negative to determine the time interval between acquisition times for symbol synchronization timings for received signals in both branches is adequately close (small time difference).

[0086] An output from decider 702 is input to selector 703 as a control signal. Selector 703 executes the control so as to output an output from averager 421 and an output from selector 601 selectively.

[0087] For example, in the case where the subtracted result is a negative value smaller than the threshold level, in other words, in the case where it is considered that the time interval between acquisition times for symbol synchronization timings for received signals in both branches is adequately close, it is considered that the timing detection accuracy is almost equal. The instruction indicative of the execution of averaging processing is provided to averager 421, and the frequency offset is obtained by the averaging processing. Selector 703 outputs a value obtained by averaging phase rotation amounts of received signals in both branches, which is output from averager 421, as the frequency offset amount.

[0088] On the other hand, when decider 702 decides that the symbol synchronization timings for received signals in both branches are not close, it is considered that the symbol synchronization timing for a received signal in either branch has a great error. Therefore, selector 703 outputs, as the frequency offset amount, an output from selector 601 which outputs, based on an output from fastest timing detection section 413, a phase rotation amount of a received signal in either branch of which the symbol synchronization timing is acquired at a faster timing than the other.

[0089] For example, in the case where the subtracted result is a negative value greater than the threshold level, in other words, in the case where it is considered that the time interval between acquisition times for symbol synchronization timings for received signals in both branches is not adequately close, it is judged that the symbol synchronization timing for a received signal in either branch has a great error. The instruction, indicative of the use of the phase rotation amount of a received signal in either branch of which the symbol synchronization timing is acquired at a faster timing than the other, is provided to selector 703. Selector 703 outputs, as the frequency offset amount, the phase rotation amount of the received signal in either branch of which the symbol synchronization timing is acquired at the faster timing than the other, which is output from selector 601.

[0090] As described above, according to this embodiment, in the case where the detected symbol synchronization timings for received signals in both branches are close, since the phase rotation amounts of receives signals in both branches are averaged and adopted as the frequency offset amount to be compensated, it is possible to improve the detection accuracy for the frequency offset amount, and further to execute accurate frequency offset compensation.

[0091] The OFDM reception apparatus of the present invention is applicable to a communication terminal apparatus such as a mobile station and a base station apparatus in a radio communication system. Since the accuracy for the symbol synchronization

BNSDOCID: <EP_____1005204A2_I_>

acquisition is thus improved, it is thereby possible to reduce errors in communications, and to improve channel qualities.

[0092] The above-mentioned explanations in the third to fifth embodiments describe about the case where the number of branches is 2, in other words, the number of branches for received signals is 2, however the present invention is applicable to the case where the number of branches is any of a plurality of numbers.

[0093] In addition, the above-mentioned explanations in the first to fifth embodiments describe about the case where the fastest timing detection section compares the counted number using the counter, however the present invention is not limited to such a case. It may be possible to apply cases other than the above-mentioned case, if it is possible in such cases to compare the timing of peak of the correlation value detected for each frame or each branch to each other, and to select the fastest timing among those to use as the symbol synchronization timing.

[0094] Further, it is possible to apply the setting method for the symbol synchronization timing described in the first and second embodiments to the case of diversity described in the third to fifth embodiments.

[0095] As described above, the OFDM reception apparatus of the present invention uses the peak detected timing for a frame of which the peak of the correlation value is detected fastest among a plurality of frames received during a predetermined time, as the symbol synchronization timing which is the timing for FFT processing initiation, and in the diversity, uses the peak detected timing for a received signal in a branch of which the peak of the correlation value is detected fastest among all received signals, as the symbol synchronization timing which is the timing for FFT processing initiation common to received signals in all branches, thereby enabling the improvement of the accuracy for the symbol synchronization acquisition, and further enabling the improvement of error rate under multipath environments.

[0096] The present invention is not limited to the above described embodiments, and various variations and modifications may be possible without departing from the scope of the present invention.

[0097] This application is based on the Japanese Patent Applications No. HEI10-336111 filed on November 26, 1998 and No. HEI11-79574 filed on March 24, 1999, entire content of which is expressly incorporated by reference herein.

Claims

1. An OFDM reception apparatus comprising:

   a timing detection section(106) which detects a symbol synchronization timing for a received signal composed of a plurality frames, for each frame;

   a timing selection section(107) which selects a fastest timing among timings which are detected in said timing detection section during a predetermined time; and

   a Fourier transform section(108) which executes Fourier transform processing on the received signal using a timing selected in said timing selection section(107) as a processing initiation timing.

2. The OFDM reception apparatus according to claim 1, wherein said timing selection section(107) having:

   a conversion section(201) which converts each timing detected in said timing detection section into a numerical value corresponding to a fastness of an occurrence time of said timing; and

   an extraction section(202) which compares a converted numerical value to each other to extract the converted numerical value corresponding to the timing detected fastest in said timing detection section.

3. The OFDM reception apparatus according to claim 1, wherein said timing selection section(107) having:

   a conversion section(201) which converts each timing detected in said timing detection section into a numerical value corresponding to a fastness of an occurrence time of said timing;

   a storage section(203) which stores converted numerical values only for a timing;

   a comparison section(204) which compares the numerical value converted in said conversion section to that read out from said storage section to output (the numerical value corresponding to) the timing detected faster than the other in said timing detection; and

   an update control section which, based on a compared result in said comparison section, updates the numerical value corresponding to the timing detected faster than the other in said timing detection section to store in said storage.

4. An OFDM reception apparatus comprising:

   a timing detection section(411,412) which detects a symbol synchronization for each of received signals received in a plurality of branches, for each branch;

   a timing selection section(413) which selects a fastest timing among timings detected in said timing detection section;

   a Fourier transform processing control section(414,415) which sets a timing selected in

BNSDOCID: <EP_____1005204A2_I_>

said timing selection section as an initiation timing common to Fourier transform processing for the received signal in each branch; and

a demodulation section(417) which selects a received signal of which a received level is highest among the received signals in respective branches subjected to the Fourier transform processing to demodulate.

5. The OFDM reception apparatus according to claim 4, wherein said timing selection section having:

a conversion section(501,502) which converts each timing detected in said timing detection section into a numerical value corresponding to a fastness of an occurrence time of said timing; and

an extraction section which compares a converted numerical value to each other to extract the converted numerical value corresponding to the timing detected fastest in said timing detection section.

6. The OFDM reception apparatus according to claim 4, further comprising:

a phase rotation amount calculation section which is provided for each branch and calculates a phase rotation amount of a received signal in each branch; and

a frequency offset compensation section which, based on the phase rotation amount of the received signal in the branch with a timing selected in said timing selection section, executes frequency offset compensation on received signals in all branches.

7. The OFDM reception apparatus according to claim 6 further comprising:

an averaging section(421) which averages phase rotation amounts of the received signals in respective branches, said amounts being output from said phase rotation amount calculation section;

a decision section which decides whether or not a difference between occurrence times for symbol synchronization timings for received signals in respective branches is more than a predetermined level, said timings being output from said timing detection section; and

a control section which, based on a decided result in said decision section, when the difference between occurrence times is equal to or more than the predetermined level, controls said frequency offset compensation section to execute frequency offset compensation on received signals in all branches based on the phase rotation amount of the received signal in the branch with the timing selected in said timing selection section, and when the difference between occurrence times is less than the predetermined level, controls said frequency offset compensation section to execute the frequency offset compensation on received signals in all branches based on the phase rotation amount subjected to averaging processing, said amount being output from said averaging section.

8. A symbol synchronization error reduction method comprising:

the timing detection step of detecting a symbol synchronization timing for a received signal composed of a plurality frames, for each frame;

the timing selection step of selecting a fastest timing among timings detected in said timing detection step during a predetermined time; and

the Fourier transform step of executing Fourier transform processing on the received signal using a timing selected in said timing selection step as a processing initiation timing.

9. The symbol synchronization error reduction method according to claim 8, wherein in said timing selection step, each timing detected in said timing detection step is converted into a numerical value corresponding to a fastness of an occurrence time of said timing, and by comparing a converted numerical value to each other, the converted numerical value corresponding to the timing detected fastest in said timing detection step is extracted.

10. The symbol synchronization error reduction method according to claim 8, wherein in said timing selection step, each timing detected in said timing detection step is converted into a numerical value corresponding to a fastness of an occurrence time of said timing, converted numerical values only for a timing are stored, a converted numerical value is compared to a stored numerical value, the numerical value corresponding to the timing detected faster than the other in said timing detection step is output, and corresponding to an output timing, the numerical value corresponding to the timing detected faster than the other in said timing detection step is updated to store.

11. A symbol synchronization error reduction method comprising:

the timing detection step of detecting a symbol synchronization for each of received signals

BNSDOCID: <EP_____1005204A2_I_>

received in a plurality of branches, for each branch;

the timing selection step of selecting a fastest timing among timings detected in said timing detection step;

the Fourier transform processing control step of setting a timing selected in said timing selection step as an initiation timing common to Fourier transform processing for the received signal in each branch; and

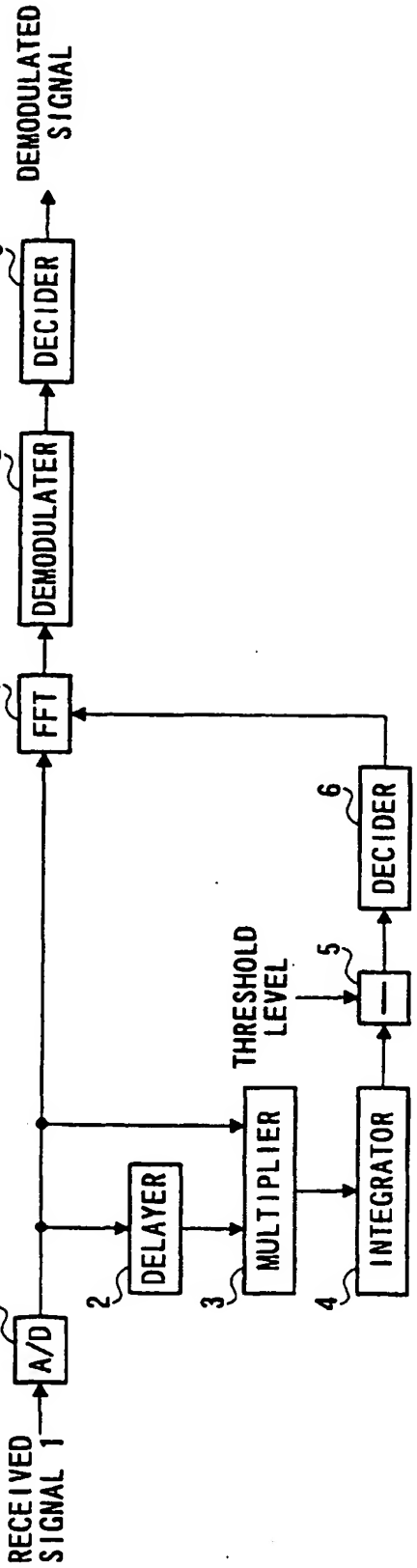
the demodulation step of selecting a received signal of which a received level is highest among the received signals in respective branches subjected to the Fourier transform processing to demodulate.

12. The symbol synchronization error reduction method according to claim 11, wherein in said timing selection step, each timing detected in said timing detection step is converted into a numerical value corresponding to a fastness of an occurrence time of said timing, and by comparing a converted numerical value to each other, the converted numerical value corresponding to the timing detected fastest in said timing detection step is extracted.

13. The symbol synchronization error reduction method according to claim 11, wherein a phase rotation amount of a received signal in each branch is calculated, and based on the phase rotation amount of the received signal in the branch with a timing selected in said timing selection step, frequency offset compensation is executed on received signals in all branches.

14. The symbol synchronization error reduction method according to claim 13, wherein phase rotation amounts of the received signals in respective branches are averaged, it is decided whether or not a difference between occurrence times for symbol synchronization timings for received signals in respective branches is more than a predetermined level, said timings being output from said timing detection step, and based on a decided result, when the difference between occurrence times is equal to or more than the predetermined level, frequency offset compensation is executed on received signals in all branches based on the phase rotation amount of the received signal in the branch with the timing selected in said timing selection step, and when the difference between occurrence times is less than the predetermined level, the frequency offset compensation is executed on received signals in all branches based on the phase rotation amount subjected to averaging processing.

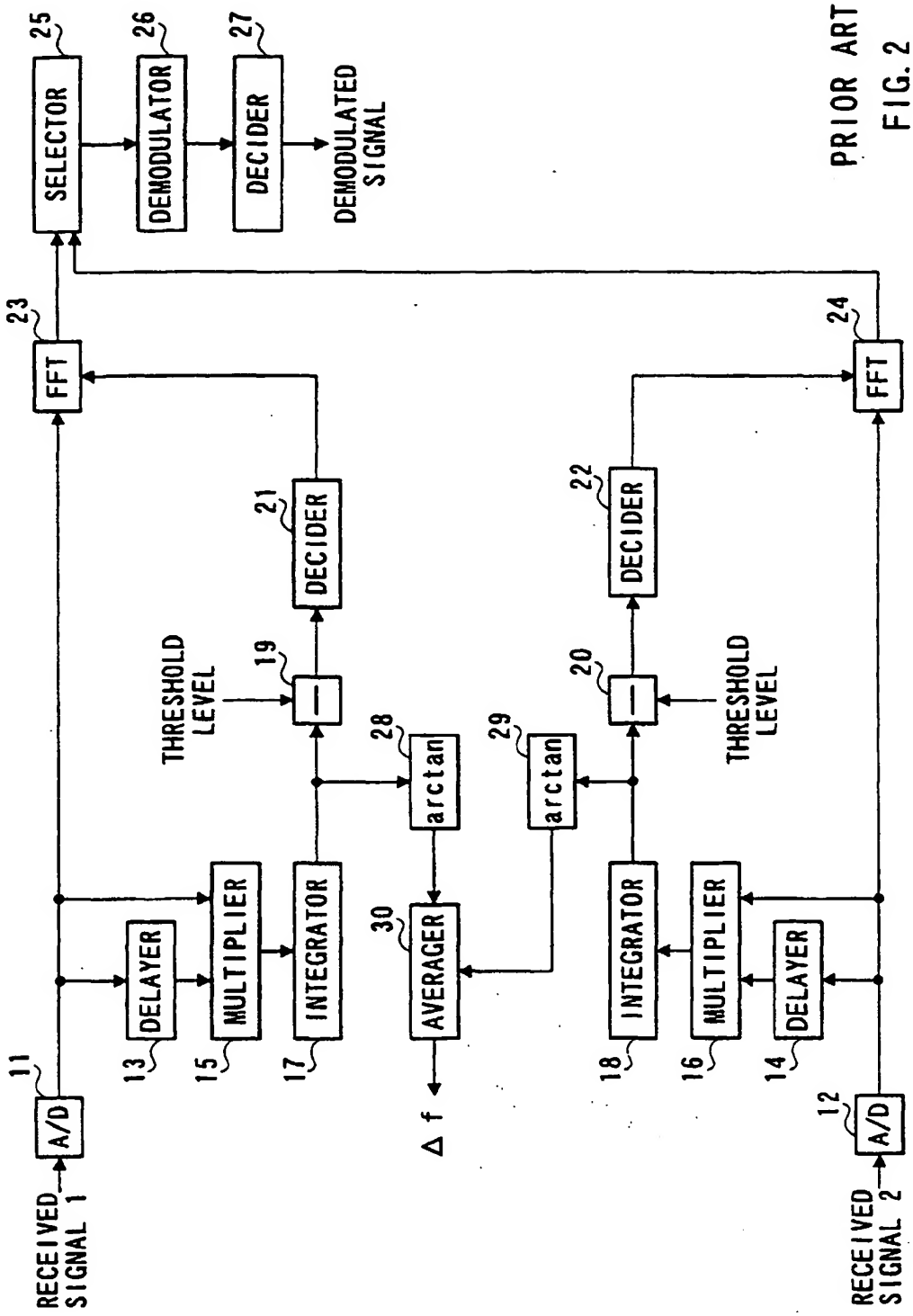
BNSDOCID: <EP_____1005204A2_I_>



PRIOR ART

FIG. 1

BNSDOCID: <EP_____1005204A2_I_>



PRIOR ART
FIG. 2

BNSDOCID: <EP_____1005204A2_I_>

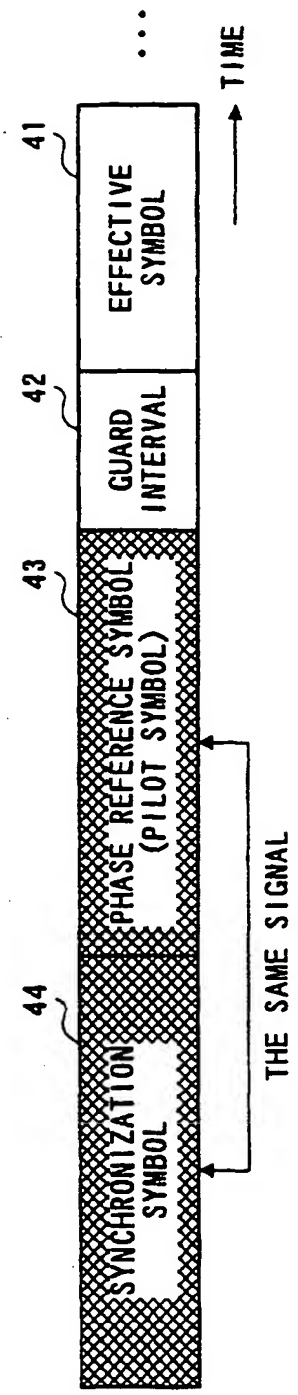


FIG. 3

BNSDOCID: <EP_____1005204A2_I_>

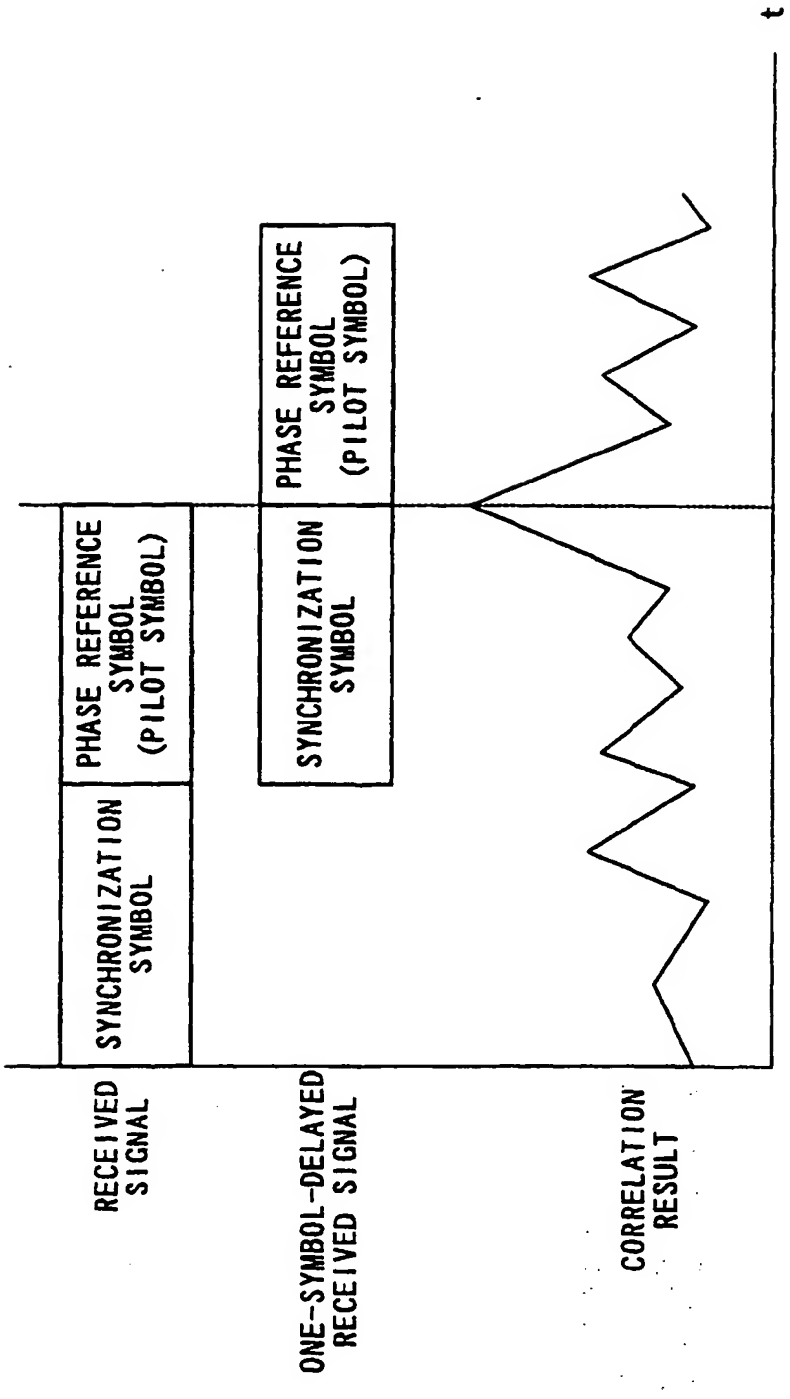


FIG. 4

EPODOC: <EP_____1005204A2_I_>

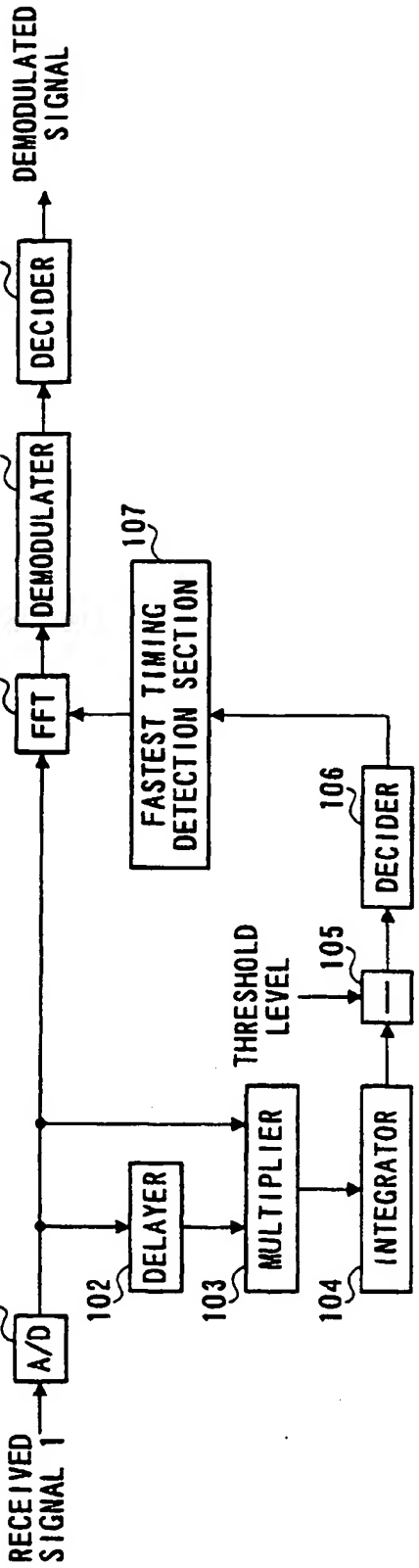


FIG. 5

BNSDOCID: <EP_____1005204A2_I_>

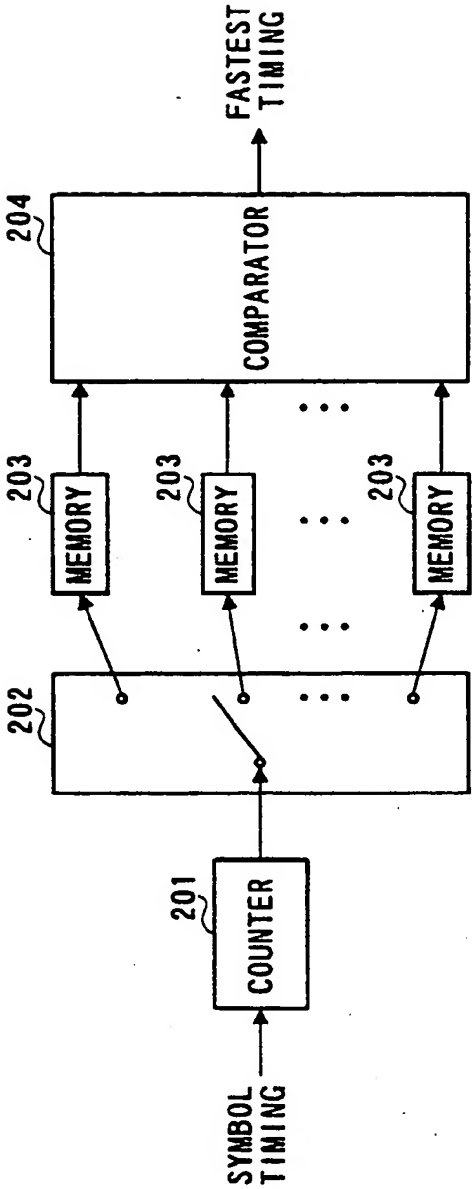


FIG. 6

EPODOC: <EP_____1005204A2_I_>

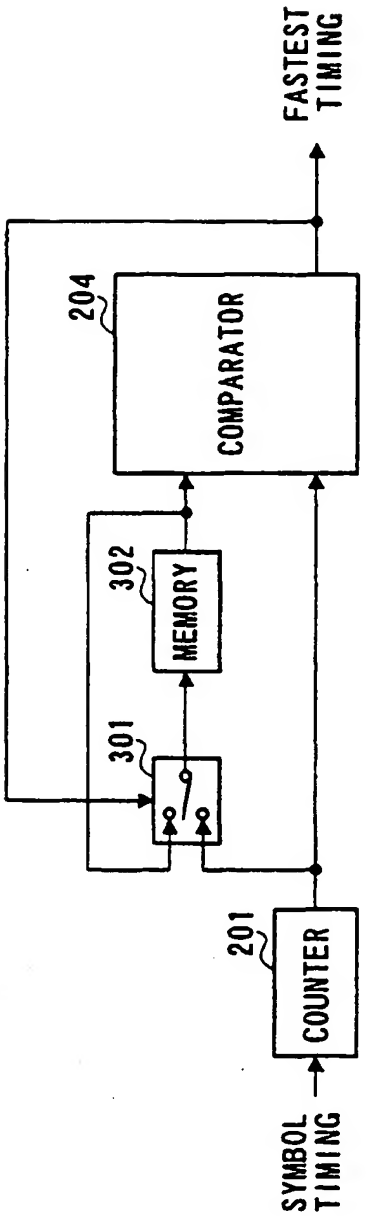


FIG. 7

BNSDOCID: <EP_____1005204A2_I_>

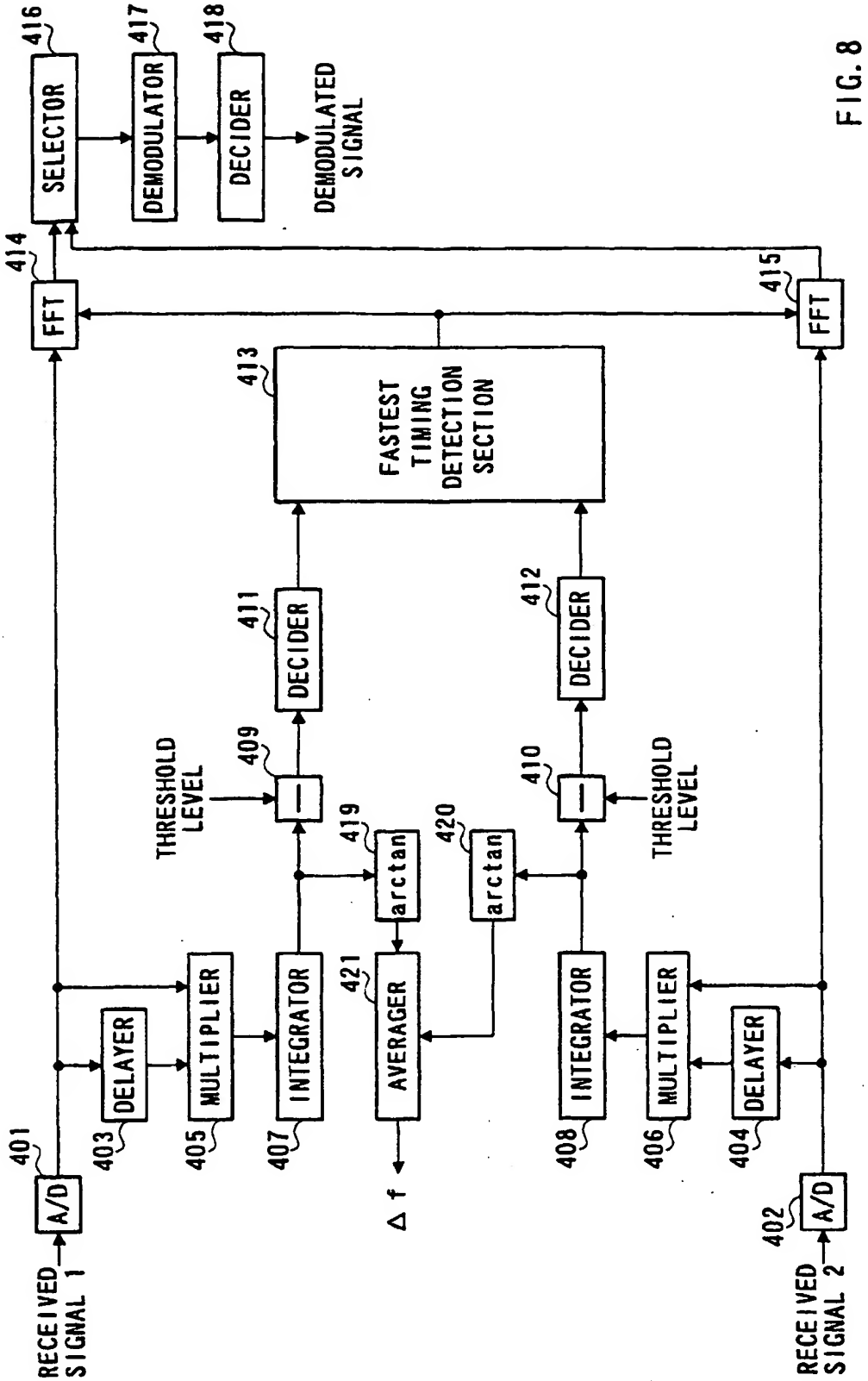


FIG. 8

BNSDOCID: <EP_____1005204A2_I_>

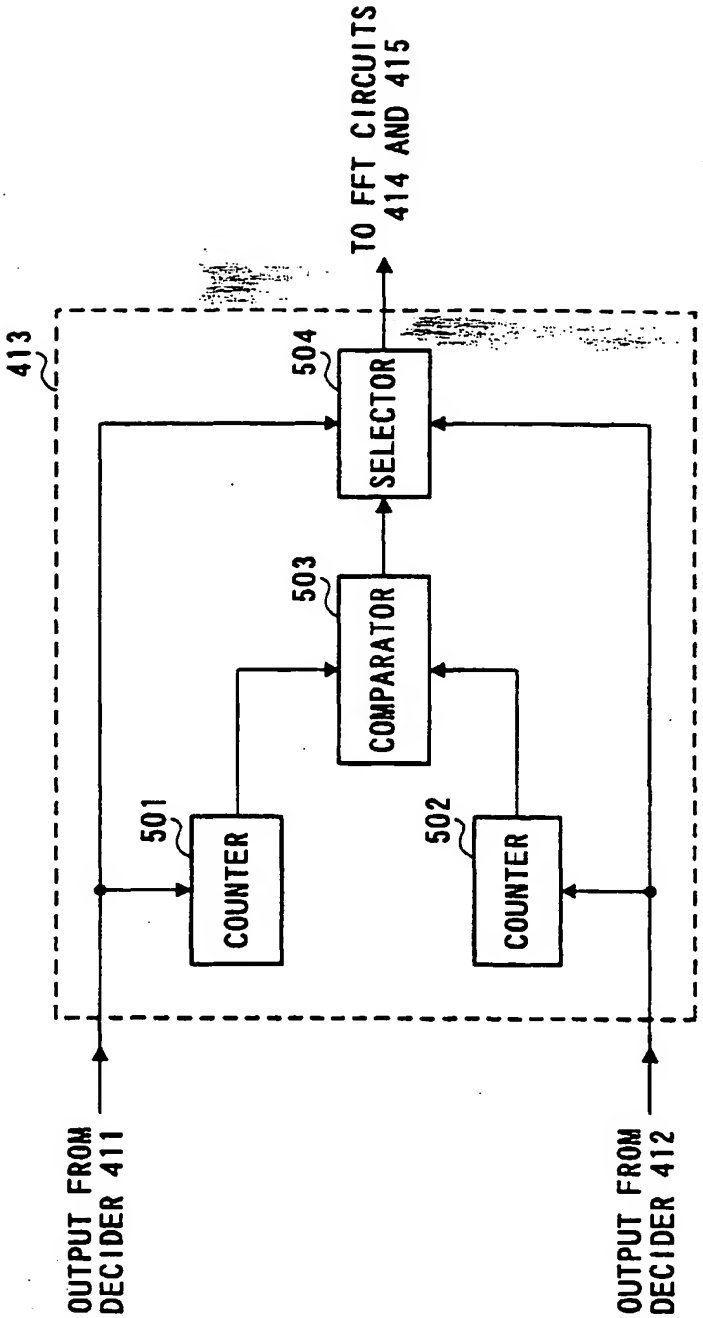


FIG. 9

BNSDOCID: <EP_____1005204A2_I_>

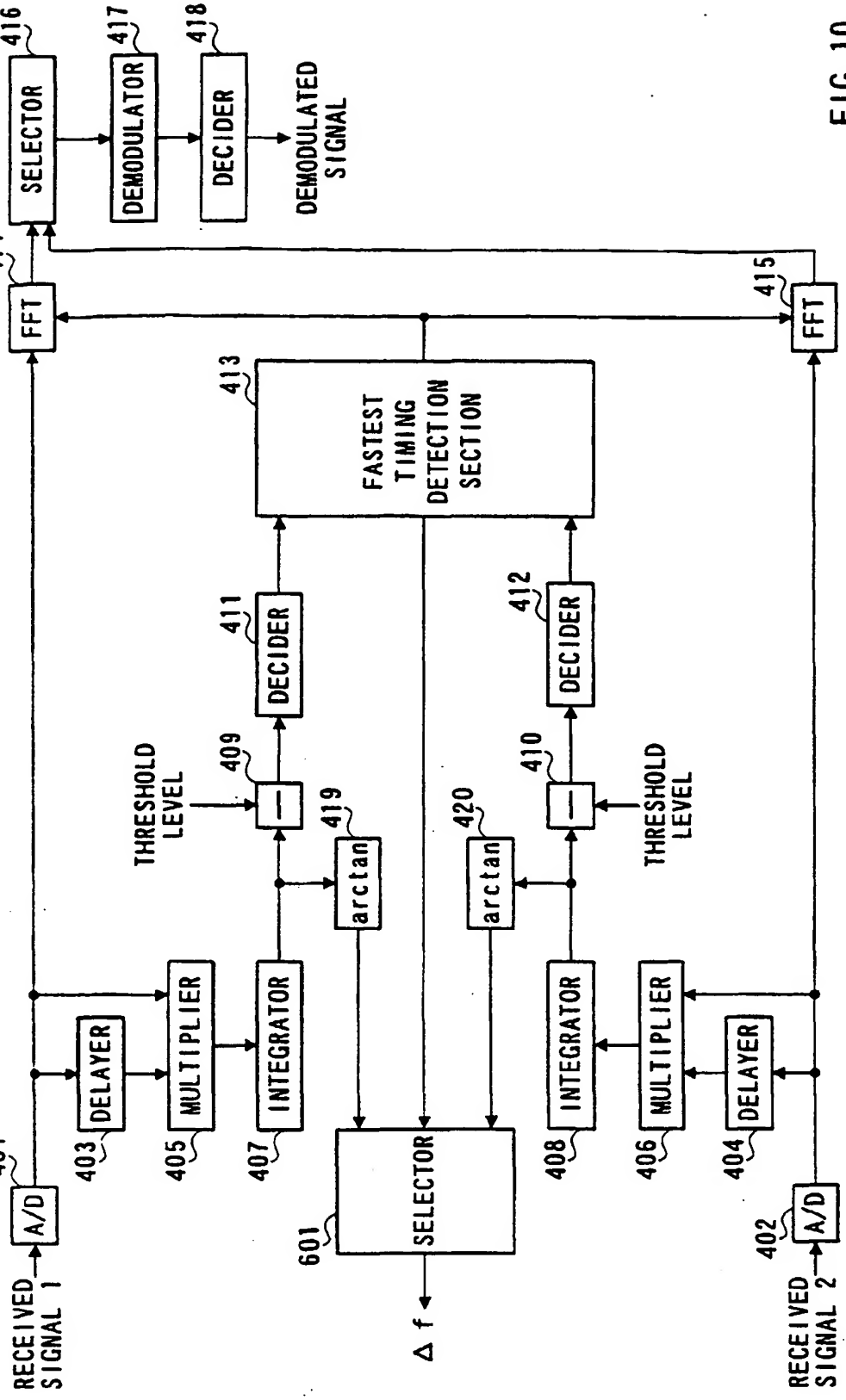


FIG. 10

BNSDOCID: <EP_____1005204A2_I_>

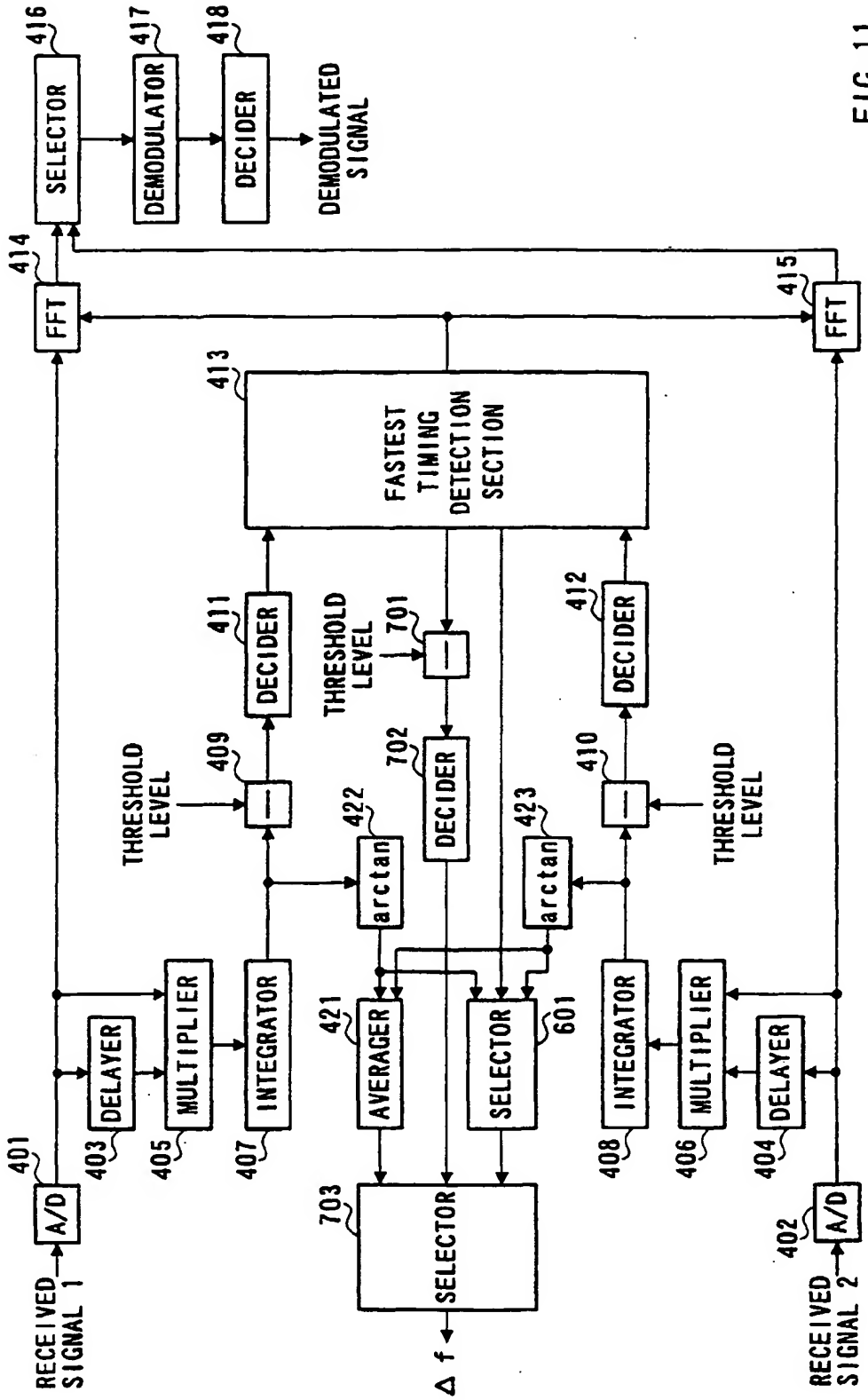


FIG. 11

BNSDOCID: <EP_____1005204A2_I_>

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 005 204 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
28.01.2004 Bulletin 2004/05

(51) Int Cl.[7]: **H04L 27/26**

(43) Date of publication A2:
31.05.2000 Bulletin 2000/22

(21) Application number: **99123430.3**

(22) Date of filing: **24.11.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.11.1998 JP 33611198**
24.03.1999 JP 7957499

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka 571-8501 (JP)

(72) Inventor: **Sudo, Hiroaki**
Yokohama-shi, Kanagawa 224-0054 (JP)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Symbol synchronization in an OFDM receiver

(57) Multiplier 103 calculates the correlation value of the received signal with the one-symbol-delayed received signal, integrator 104 integrates the calculated correlation value, subtracter 105 executes subtract processing between the integrated value and an arbitrary threshold level, and decider 106 decides a level of the resultant, fastest timing detection section 107 compares the peak detected timing for each of a plurality of frames received during a predetermined time to each other to select the fastest peak detected timing, and using the selected timing as a processing initiation timing, FFT circuit 108 executes FFT processing on the received signal.

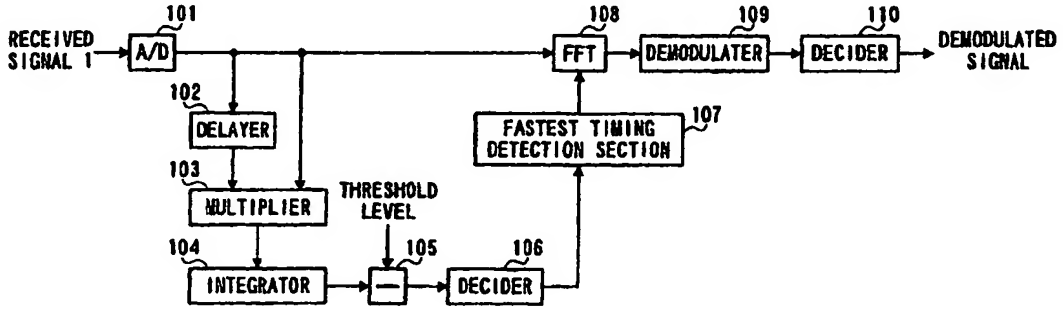


FIG. 5

EP 1 005 204 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 12 3430

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 854 620 A (SONY CORP) 22 July 1998 (1998-07-22) * column 8, line 23 - column 10, line 43; figures 5,6A-6F *	1-14	H04L27/26
A	EP 0 876 025 A (SONY CORP) 4 November 1998 (1998-11-04) * column 10, line 48 - column 18, line 51; figures 1,7-10 *	1-14	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04L
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	5 December 2003	Marzenke, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

BNSDOCID: <EP_____1005204A3_I_>

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 12 3430

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

05-12-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0854620 A	22-07-1998	JP 10209998 A	07-08-1998
		CA 2227102 A1	28-07-1998
		EP 0854620 A2	22-07-1998
		US 6108353 A	22-08-2000
EP 0876025 A	04-11-1998	JP 10308713 A	17-11-1998
		AU 734249 B2	07-06-2001
		AU 6376098 A	05-11-1998
		EP 0876025 A1	04-11-1998
		US 5920598 A	06-07-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

BNSDOCID: <EP_____1005204A3_I_>